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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/715,743	11/17/2003	Edward Y. Chang	WPG-001	4380

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EXAMINER	
SARKAR, ASOK K	

ART UNIT	PAPER NUMBER
2829	

DATE MAILED: 08/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/715,743	CHANG ET AL.	
	Examiner	Art Unit	
	Asok K. Sarkar	2829	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-11* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☒ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/29/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Acknowledgment is made of applicant's claim for foreign priority based on an application filed in Taiwan on 5/13/2003. It is noted, however, that applicant has not filed a certified copy of the 092112920 application as required by 35 U.S.C. 119(b).

Claim Objections

2. Claim 1 is objected to because of the following informalities: In step (iv), line 15, the phrase "... recess on the gate;" should be replaced by "... recess of (or for) the gate;". Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of

the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1 – 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anda, US 6,051,454 in view of Hatada, US 4,523,000; Okoroanyanwu, US 6,767,693 and Yoshida, US 5,712,175.

Regarding claim 1, Anda teaches a method for fabricating nanometer gate semiconductor device comprising the following steps:

- (i) coating two layers of photoresists on a substrate, where a bottom layer of photoresist, one of said two layers of photoresists, is a polymeric photoresist which has a lower sensitivity and a higher resolution with respect to an electron beam, and a top layer of photoresist, one of said two layers of photoresists, is another polymeric photoresist which has a higher sensitivity and a lower resolution with respect to the electron beam;
- (iii) using photolithography with a high accelerating voltage in an electron beam direct writing manner to expose a pattern on said two layers of photoresists for forming a gate (inherent in the process);
- (iv) using a developer and an etchant for developing and etching in order to form a recess on the gate; These steps are inherent in the process.

- (v) plating a metallic layer on the recess of the gate by way of using an electron gun evaporation technique; and
- (vi) removing said photoresists to obtain the gate with respect to Figs. 8(a) – 8(d) and 9(a) – 9(c) in between column 1, line 45 to column 2, line 32.

Anda fails to teach (1) coating two layers of photoresists on a substrate by spin coating, (2) heating said two layers of photoresists for curing by way of using a hotplate and (3) after the etching of the recess of the gate, the photoresists are reflowed by using a hot plate heating manner within a predetermined period of time and temperature, such that the recess of the gate is formed with a nanometer-sized width.

Regarding elements (1) and (2), Hatada teaches spin coating as a typical way to apply the resist and heating (prebaking) the resist layer for the benefit of increasing the adhesiveness to the substrate in column 8, lines 9 – 25. Hatada does not mention using the hotplate.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Anda and use spin coating as a typical way to apply the resist and heating (prebaking) the resist layer for the benefit of increasing the adhesiveness to the substrate as taught by Hatada in column 8, lines 9 – 25. it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Anda and use a hotplate for heating the resist layers for curing since hotplate is a heating device typically used in a laboratory set up for routine heating purposes.

Regarding element 3, Okoroanyanwu teaches that photoresists can be modified by a heating process for the benefit of achieving sublithographic resolution to reduce the size of contact holes in column 2, lines 11 – 24.

Yoshida teaches a resist reflow process for the benefit of rounding corners of the gate pattern to avoid disconnection while forming the mushroom type gate electrode with reference to Fig. 6 in column 4, lines 4 – 10. Yoshida teaches also the time and temperature for the process in column 4, lines 4 – 10.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Anda and use photoresists reflow process such that the recess of the gate is formed with a nanometer-sized width for the benefit of achieving sublithographic resolution to reduce the size of contact hole as taught by Okoroanyanwu in column 2, lines 11 – 24 and also for the benefit of rounding corners of the gate pattern to avoid disconnection while forming the mushroom type gate electrode as taught by Yoshida in column 4, lines 4 – 10. It would have been obvious also to one with ordinary skill in the art at the time of the invention to modify Anda and use a hot plate heating manner within a predetermined period of time and temperature since hotplate is a simple device for heating samples and judiciously adjust and control time and temperature through routine experimentation and optimization (in order to avoid excessive deformation) to achieve optimum benefits (see MPEP 2144.05) in terms to shrinking the hole size to a nanometer-sized width.

Regarding claims 2, 3 and 11, Anda teaches PMMA photoresists in column 1, lines 48 – 52.

Regarding claim 4, Anda teaches Ti/Pt/Au Schottky metallic layer in column 10, line 20.

Regarding claims 5 and 6, Anda in view of Hatada, Okoroanyanwu and Yoshida fails to teach the temperature and time for the reflow and the heating temperatures for the photoresist layers.

However, it would have been obvious to one with ordinary skill in the art at the time of the invention to judiciously adjust and control these parameters during the resist curing and the reflow process through routine experimentation and optimization to achieve optimum benefits (see MPEP 2144.05) and it would not yield any unexpected results.

Note that the specification contains no disclosure of either the critical nature of the claimed processes or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen methods or upon another variable recited in a claim, the Applicant must show that the chosen methods or variables are critical (*Woodruff*, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir., 1990)). See also *In re Aller, Lacey and Hall* (10 USPQ 233 – 237).

Regarding claim 7, Hatada teaches that PMMA copolymers can be dissolved by acetone in column 7, line 28 and therefore acetone can be used to remove photoresists.

Regarding claim 8, Anda teaches T-shaped gate with reference to Fig. 1.

Regarding claim 9, Anda teaches GaAs substrate in column 7, line 49.

Regarding claim 10, Anda teaches developer MIBK:IPA in column 9, lines 57 – 60.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Inai, US 2003/0129818 teaches a method for forming T-gate by resist reflow process

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Tokar can be reached on 571 272 1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Asok Kumar Sarkar

Asok K. Sarkar
August 16, 2004

Patent Examiner